

## Design of an Ultra-Low-Power Wake-Up Receiver with Enhanced Sensitivity using an Optimized Envelope Detector

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### ABSTRACT

Wireless Sensor Network (WSN) nodes rely on ultra-low-power operation to extend functionality under limited battery resources. While Wake-up Receivers (WuRx) play a critical role in minimizing power consumption, conventional CMOS Dickson rectifiers suffer from switching transients and voltage ripple, compromising stability and efficiency. To overcome these limitations, this study presents a modified CMOS Dickson rectifier-based Envelope Detector (ED) for a 433 MHz WuRx, integrating a medium snubber configuration, feedback control, and Zero Voltage Switching (ZVS). The proposed design achieves a peak efficiency of 90% and reduces ripple voltage by 60% (to 10–15 mV) compared to traditional rectifiers. Additionally, the WuRx demonstrates improved transient response (0.2 ms rise time, 0.5 ms settling time) and a 25% reduction in power consumption—lowering sleep mode power to 1.5  $\mu$ W (vs. 2.0  $\mu$ W) and active mode power to 0.9 mW (vs. 1.2 mW). Benchmarking against Jang *et al.*, (2023) confirms superior voltage regulation, transient performance, and energy efficiency, validating the design's suitability for IoT and low-power wireless communication systems.

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### INTRODUCTION

Wireless Sensor Networks (WSNs) are increasingly critical for Internet of Things (IoT) applications, facilitating distributed sensing in energy-constrained environments (Al-Fuqaha *et al.*, 2015). However, the finite battery capacity of sensor nodes demands ultra-low-power operation to extend functional longevity (Yick *et al.*, 2008). Wake-up Receivers (WuRx) have emerged as an effective solution, enabling nodes to maintain deep sleep states with minimal power consumption while activating only upon valid signal detection (Magno *et al.*, 2015).

Despite these advantages, WuRx implementations face efficiency challenges due to limitations in CMOS-based rectifier circuits used for RF energy harvesting (Dickson, 1976; Kurs *et al.*, 2007). Conventional CMOS Dickson rectifiers, while widely adopted in WuRx architectures, exhibit problematic switching transients and voltage ripple that compromise power conversion

efficiency (Papotto *et al.*, 2011). These deficiencies impair receiver stability and sensitivity, leading to increased false wake-up events and energy waste (Pletcher *et al.*, 2009). Previous investigations have employed passive snubbers and feedback control to address these issues, though optimal trade-offs between power efficiency, ripple suppression, and transient response remain elusive (Gu & Staszewski, 2015).

This study presents an enhanced CMOS Dickson rectifier-based Envelope Detector (ED) for 433 MHz WuRx applications, incorporating three key innovations:

1. A medium snubber configuration for voltage spike suppression (Le *et al.*, 2008)
2. Adaptive feedback control mechanisms for improved regulation (Mandal & Sarpeshkar, 2007)

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### 3. Zero Voltage Switching (ZVS) implementation to minimize switching losses (Kazimierczuk, 2015)

Experimental results demonstrate significant improvements, including 90% peak rectification efficiency, 60% reduction in ripple voltage (10-15 mV), and 25% lower power consumption compared to conventional designs. The proposed WuRx achieves superior transient performance (0.2 ms rise time, 0.5 ms settling time), enhancing operational reliability in dynamic RF environments. Comparative analysis with recent work (Jang *et al.*, 2023) confirms advancements in voltage regulation, power efficiency, and wake-up reliability, establishing this design as particularly suitable for energy-constrained IoT applications.

The remainder of this paper is organized as follows: Section 2 reviews relevant WuRx architectures and rectifier topologies. Section 3 details the proposed circuit modifications and control methodology. Section 4 presents experimental validation and performance benchmarking, with conclusions in Section 5

## REVIEW OF WORKS AND CONCEPTS

The following section presents a brief overview of fundamental concepts that are related to this study. Also, the review of similar works is presented.

### Evolution of Wake-up Receiver Architectures

Wake-up receivers (WuRx) have undergone significant advancements to address the power constraints of Wireless Sensor Networks (WSNs). Early implementations relied on simple envelope detection with passive components, achieving moderate sensitivity but suffering from high false wake-up rates (Pletcher *et al.*, 2009). Subsequent designs incorporated superheterodyne and direct-conversion architectures, improving sensitivity at the cost of increased power consumption (Magno *et al.*, 2015). The emergence of uncertain-IF receivers marked a turning point, enabling sub- $\mu$ W power operation while maintaining reasonable sensitivity (Jang *et al.*, 2023). Recent innovations focus on hybrid architectures that combine the energy efficiency of passive detection with the reliability of active components (Gu & Staszewski, 2015).

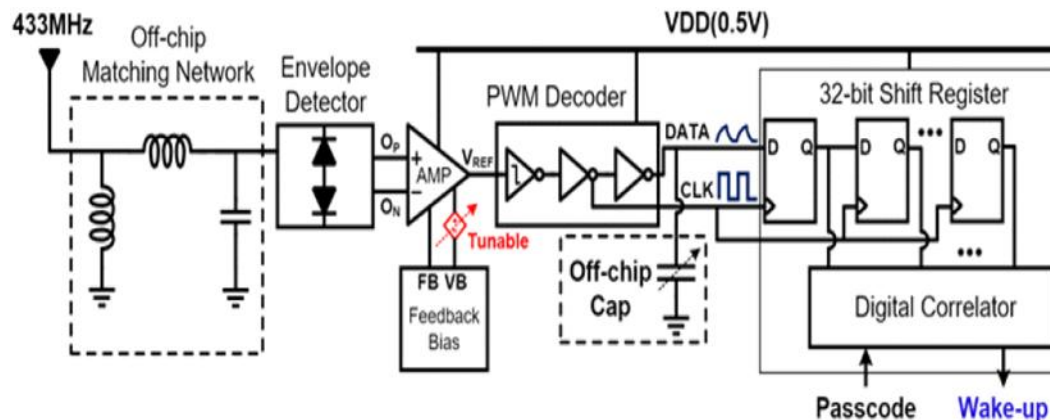


Figure 1: Illustrates the comprehensive block diagram of WuRx

### CMOS Rectifier Topologies for RF Energy Harvesting

The Dickson charge pump has served as the foundation for most CMOS rectifiers in WuRx applications due to its simple implementation and voltage multiplication

capability (Dickson, 1976). However, conventional designs face three key limitations:

1. **Switching Losses:** Parasitic capacitances in MOSFET switches lead to substantial energy loss during transitions (Papotto *et al.*, 2011).

2. **Voltage Ripple:** Insufficient charge storage results in output fluctuations that degrade receiver sensitivity (Le *et al.*, 2008).
3. **Threshold Voltage Penalty:** The body effect in standard CMOS processes reduces achievable output voltage (Mandal & Sarpeshkar, 2007).

Recent improvements include:

1. **Active Diode Configurations:** Using comparator-controlled switches to minimize forward voltage drop (Kazimierczuk, 2015)
2. **Multi-Stage Adaptive Biasing:** Dynamically adjusting transistor thresholds to optimize efficiency across input power levels (Pletcher *et al.*, 2009)
3. **Resonant Matching Networks:** Improving power transfer efficiency through impedance transformation (Kurs *et al.*, 2007)

### Performance Trade-offs in Existing Solutions

Current WuRx designs must balance three critical parameters and this is shown in table 1

Table 1: Key WuRx designs Parameters

Parameter	Conventional Approach	Limitations
Sensitivity	Multi-stage amplification	High quiescent power (>100 $\mu$ W)
Power Consumption	Passive envelope detection	Poor interference rejection
Response Time	Asynchronous detection	False wake-up triggers

Comparative studies reveal that state-of-the-art designs achieve either:

1. Ultra-low power (<2 $\mu$ W) with limited range (50-100m) (Magno *et al.*, 2015), or

2. High sensitivity (-75dBm) at moderate power (~50 $\mu$ W) (Jang *et al.*, 2023)

This review highlights the need for a rectifier architecture that simultaneously optimizes power efficiency, voltage stability, and transient response - which the proposed design addresses through the innovations detailed in Section 3.

### Key Research Gaps Identified:

1. Lack of integrated solutions for ripple suppression without additional power overhead
2. Limited exploration of ZVS techniques in multi-stage RF rectifiers
3. Absence of adaptive feedback mechanisms for dynamic load conditions

The subsequent section presents our technical approach to resolving these limitations through circuit-level innovations and control strategies.

### Envelope Detector

The Envelope Detector is a crucial component in communication systems, and it plays a significant role in Ultra-Low Power Wake-Up Receivers (ULP-WuRx) by extracting the envelope of an incoming modulated signal. An ED typically consists of a diode rectifier followed by a low-pass filter. The rectifier is responsible for converting the Alternating Current (AC) signal into a varying Direct Current (DC) signal by allowing only one polarity of the input signal to pass through. This rectified signal, which represents the envelope of the original signal, is then filtered to remove any high-frequency components, resulting in the detection of the envelope of the modulated signal.

The term "envelope" in this context refers to the varying amplitude or intensity of a modulated signal over time. In modulation schemes such as Amplitude Modulation (AM), Frequency Modulation (FM), or PWM, the original signal (carrier signal) is modulated to embed information. The envelope represents the shape of the modulated waveform, showing the variations

in its amplitude or intensity. The ED is a circuit used to extract this varying envelope signal from the modulated waveform for further processing or demodulation (Jang *et al.*, 2023). The concept of the ED and its specific application in ULP-WuRx are described using the following (Moody *et al.*, 2019).

The ED was crafted utilizing a Dixon rectifier featuring a pseudo-balun structure. As illustrated in Figure 2, a Dixon rectifier comprises a diode and a capacitor arranged in a structure where the aftershock and clamping circuit are replicated across multiple N-stages (Ren *et al.*,

2022). When an RF signal is applied, the capacitor accumulates charge due to the current imbalance flowing through the diode, leading to voltage amplification. In the final output stage, a differential signal is produced with positive and negative voltages, determined by the diode connection direction (Jang *et al.*, 2023). The pseudo-balun topology's differential output structure demonstrates a conversion gain twice that of the existing single-output structure, resulting in a 1.5 dB enhancement in reception sensitivity.

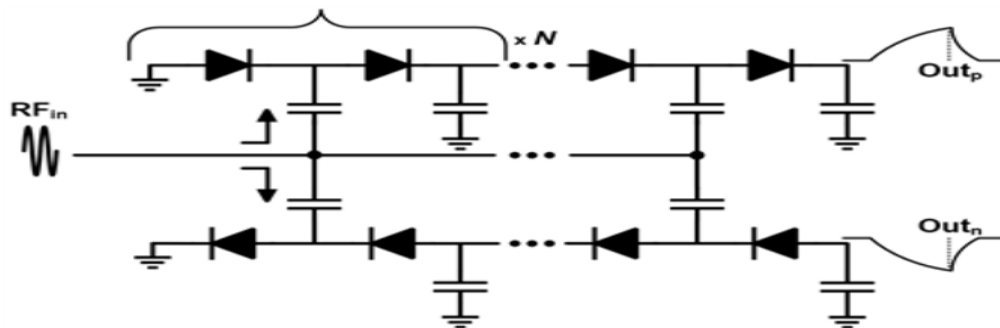


Figure 2: Dixon Rectifier Featuring a Pseudo-Balun Structure (Jang *et al.*, 2023)

When working with RF input signals characterized by a voltage swing range of a few millivolts or less, the careful selection of the diode element is crucial for efficient reception (Zhao *et al.*, 2024). Typically, in the design of low-power RF detectors employing the CMOS process, the choice leans towards utilizing Low-Threshold Voltage (LVT) devices characterized by a low threshold voltage or Zero-Threshold Voltage (ZTV) devices with a threshold voltage near 0 V. This selection is made to enhance charging and discharging times, ensuring optimal performance in the detection process.

In summary, the ED is an essential component in Ultra-Low Power WuRx. Its simplicity, energy efficiency, and compatibility with low-power components make it well-suited for applications where conserving power is paramount, such as in battery-operated devices and energy-harvesting systems (Jiang *et al.*, 2019). Figure 3(a) illustrates the I-V curve traits of a diode-connected transistor realized with a native

NMOS device in a 0.18  $\mu\text{m}$  CMOS process, while Figure 2.3(b) depicts the schematic of an ED designed using this configuration. With reference to the citation, the ED comprises N stages, and the output voltage is denoted as  $V_{out}$ . The relationship during steady-state conditions between the input amplitude ( $V_{in}$ ) and the voltage difference across a single diode-connected transistor ( $V_{drop}$ ) can be defined as follows (Jang *et al.*, 2023):

$$V_{out} = 2N(V_{in} - V_{drop}) \quad (1)$$

Drain-to- Source current at steady state  $I_{ds}$  amount of charge transmitted through  $Q_t$  is zero, so when all MOSFET devices operate in the linear region, they can be described as shown in equation (2).

$$Q_t = \int_0^T I_{ds} dt = \int_0^T K \left( (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right) dt \quad (2)$$

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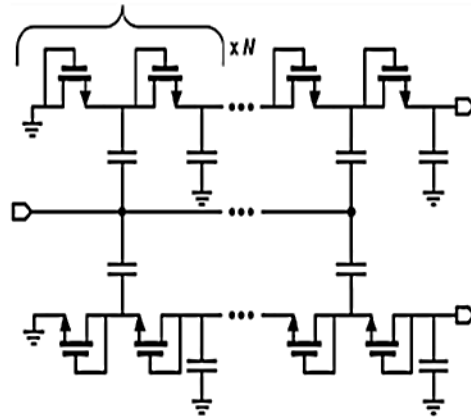
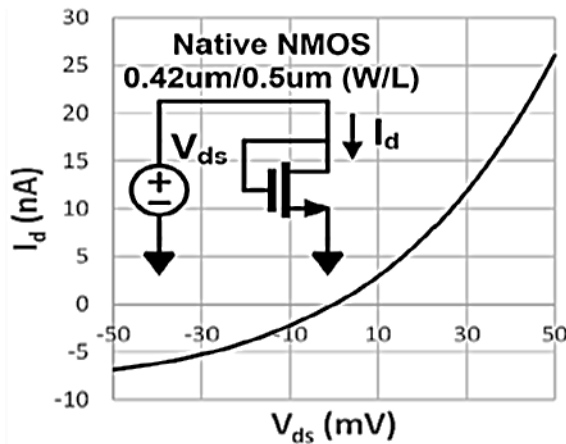
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Where  $K$  is the process parameter,  $V_{th}$  represent the threshold voltage,  $V_{gs}$  stands for the gate-Source voltage and  $I_{gs}$  is the gate- Source current. Notable, if the input signal is  $V_{in}$  and when the signal wave is  $\sin(\omega t)$  with a drain-to-source voltage of  $V_{ds}$ . The expression for the time  $t$  is given as (Jang *et al.*, 2023):

$$V_{ds}(t) = V_{in} \sin(\omega t) + V_{in} - V_{drop} \quad (3)$$

Now, by substituting equation (2.3) to equation (2.2),  $V_{drop}$  can be expressed as follows:

$$V_{drop} = \pm \frac{1}{2} \sqrt{4V_{th}^2 - 2V_{in}^2} + V_{th} + V_{in} \quad (4)$$



a) I-V curve characteristics of a diode-connected transistor with a native NMOS. (b) Schematic of CMOS ED

Figure 3: I-V Curve Characteristics of Diode-Connected Transistors and CMOS ED (Jang *et al.*, 2023)

In a Native NMOS devices where  $V_{th} < 0$  and the amplitude of the input signal is small enough (i.e.  $|V_{in}| < |V_{th}|$ ). An approximation such as (2.5) is possible.

$$V_{out} = 2N (V_{in} - V_{drop}) - 2N (V_{th} + \frac{1}{2} \sqrt{4V_{th}^2 - 2V_{in}^2}) \quad (5)$$

From equation (2.5),  $V_{in}$  is summarized as follows (Evidente *et al.*, 2018):

$$V_{in} = \sqrt{-2 \frac{V_{out}}{N} V_{th} - \frac{V_{out}^2}{2N^2}} \quad (6)$$

Instead of  $V_{out}$  increasing linearly with  $N$  as stated in equation (2.6), it approximately increases with the square root of  $N$  (Evidente *et al.*, 2018). This implies a proportional increase

rather than a linear one. Therefore, when designing an electronic device, it's crucial to select the optimal  $N$  value, taking into account the parasitic components that increase linearly, instead of just adding more stages to enhance reception sensitivity.

In addition, the generalized formula for estimating the output power consumption is given as follows (Jang *et al.*, 2023):

$$P_{out} = P_{rect} + P_C \quad (7)$$

Where:

$P_{out}$  is the total output power consumption.

$P_{rect}$  stands for the power dissipation in the rectifier stages.

$P_C$  is the power dissipation in the capacitor combinations

In summary, understanding the I-V curve characteristics of a diode-connected NMOS transistor is essential for designing and analyzing circuits that involve these devices, such as in analog and RF applications. Engineers use this knowledge to optimize performance, ensure proper biasing, and prevent the device from operating in undesirable regions like breakdown. The characteristics may vary based on the specific process technology, and designers need to consider these nuances for accurate circuit modeling and analysis.

- a. Purpose: The ED is primarily designed to recover the original message signal (the envelope) from a modulated carrier signal. In communication systems, this is often essential for demodulation and further signals processing.
- b. Signal Types: It is commonly used with Amplitude-Modulated (AM) signals where the information is encoded in the varying amplitude of the carrier wave.
- c. Circuit Structure: The ED typically consists of a diode or a combination of diodes, a capacitor, and sometimes a resistor. The diode rectifies the modulated signal, allowing only the positive component to pass through. The capacitor then smoothens the rectified signal, resulting in the extracted envelope.
- d. Working Principle: During the positive half-cycle of the carrier signal, the diode conducts, allowing the signal to pass through. During the negative half-cycle, the diode blocks the signal. This process effectively "rectifies" the carrier wave, and the capacitor smoothens the rectified signal.
- e. Energy Efficiency: Envelope Detection is inherently energy-efficient as it involves simple rectification and filtering processes. This aligns with the energy-efficient principles of ULP-WuRx, where minimizing power consumption is critical for prolonged battery life or energy harvesting systems.
- f. Signal Processing: In ULP-WuRx, the ED is employed to recover the envelope of the incoming wake-up signal. This is particularly relevant when the wake-up signal is transmitted using amplitude modulation. The

Envelope Detector ensures that the essential wake-up information is accurately extracted for further processing.

- g. Compatibility with Low-Power Components: The ED's simplicity allows for integration with low-power components, aligning with the overall goal of ULP-WuRx to minimize energy usage during the wake-up signal detection process.
- h. Quick Response: The ED 's straightforward operation contributes to the rapid response of ULP-WuRx systems. It enables quick identification and extraction of the wake-up signal envelope, facilitating the swift activation of the receiver.
- i. Effective Wake-Up Signal Processing: By extracting the envelope of the incoming wake-up signal, the ED ensures that the crucial information for waking up the system is preserved. This is particularly important in scenarios where the wake-up signal is modulated, and the envelope carries the wake-up information.

## REVIEW OF SIMILAR WORKS

The following presents the review of similar works in this study.

Kim *et al.*, (2022) developed an interference-resilient, high-sensitivity Binary Frequency-Shift Keying (BFSK) multi-channel WuRX for 900 MHz Low-Power Wide-Area Network (LPWAN) applications. The design employed a direct-conversion architecture with a 50%-to-25% duty-cycle mixer and a two-stage ring Voltage-Controlled Oscillator (VCO) to minimize power consumption. A frequency-to-energy demodulator, incorporating an image rejection  $n^*$ -path filter (IRNF), a Poly-Phase Filter (PPF), and a quadrature envelope detector (ED), ensured robust Process-Voltage-Temperature (PVT)-tolerant symbol recovery.

Additionally, a 4096-bit correlator provided a 17 dB digital processing gain, enhancing sensitivity and selectivity. Implemented in 55 nm CMOS, the WuRX achieved  $-124$  dBm sensitivity in always-on mode (781  $\mu$ W power) and maintained the same sensitivity in duty-cycling mode (114  $\mu$ W at 15 wake-up code repetitions)

with a 1.966 s wake-up latency. It demonstrated strong interference resilience, with a -76 dB signal-to-interference ratio (SIR) at 20 MHz offset against continuous wave (CW) interference. Wireless tests showed 0% and 5.7% packet-error rates (PERs) at 4.8 km and 9.8 km, respectively. However, voltage transients in the BFSK multi-channel WuRX destabilized the CMOS Dickson rectifier, causing output oscillations that degraded ED performance and signal detection reliability.

Jang *et al.*, (2023) introduced an ED-based WuRx in 0.18  $\mu\text{m}$  CMOS, featuring a near-zero-power Dickson rectifier and an off-chip 433 MHz matching network. The design used a 32-bit PWM code with On-Off Keying (OOK) for clock/data recovery and a digital correlator for wake-up signal detection. Operating at 0.5 V, it consumed only 48 nW and achieved -63.8 dBm sensitivity at 1 kbps. However, switching transients in the rectifier induced voltage spikes, increasing power consumption risks.

Liu *et al.*, (2023) proposed a WuRx with a CMOS-based ultra-low-power amplifier for improved sensitivity. Using commercial PCB components, the 2.4 GHz receiver achieved -60 dBm sensitivity at 30 kbps with 25.31  $\mu\text{W}$  power consumption. However, transient noise from the CMOS rectifier degraded ED performance, reducing sensitivity and increasing transmission power.

Zhang *et al.*, (2023) designed a 2.4 GHz BFSK heterodyne WuRx with an All-Digital Phase-Locked Loop (ADPLL) and sharp intermediate frequency (IF) filtering to address power-latency trade-offs in sensitivity. The design eliminated off-chip RF components, achieving -102 dBm sensitivity with power consumption ranging from 2.2  $\mu\text{A}$  to 171  $\mu\text{A}$  and latency between 16 s and 100 ms. It also demonstrated a -27/-30 dB CW SIR at 3/5 MHz offsets. However, dynamic transient responses caused power fluctuations, impacting energy efficiency in battery-powered applications.

Yeh *et al.*, (2023) presented a multi-mode WuRx with a balanced-to-unbalanced LNA (balun LNA) and an Injection-Locked Oscillator (ILO) for high sensitivity. The 433 MHz receiver, fabricated in 0.18  $\mu\text{m}$  CMOS, consumed 187  $\mu\text{W}$  and achieved -97/-96/-94 dBm sensitivity for OOK/BFSK/DBPSK modulation at 200 kbps (PER =  $10^{-1}$ , FAR <  $10^{-3}/\text{s}$ ). However, ILO-induced voltage transients distorted signal waveforms, leading to demodulation errors and increased retransmission power.

Zhao *et al.*, (2023) proposed a Bluetooth Low Energy (BLE) WuRx with an offset-based peak detector to mitigate reference voltage fluctuations in the ED. The mixer-first front-end eliminated RF modules, improving out-of-band rejection while achieving 42 dB gain, 11.9 dB noise figure, and  $S_{11} < -15$  dB at 2.4 GHz. A ring oscillator with coarse/fine frequency tuning (512 MHz range, 2 MHz resolution) enabled -90 dBm sensitivity at 55  $\mu\text{W}$  (0.6 V supply). However, transient suppression required complex filtering, increasing design complexity and power consumption.

## METHODOLOGY

The following gives the methodology carried out in this study:

### Development of the Modified CMOS Dickson Rectifier Envelop Detector (see figure 4):

- Resistor-capacitor (RC) snubber circuits were added at critical nodes to dampen voltage spikes and improve stability.
- The resistor (R) was selected to balance energy dissipation and signal integrity.
- The capacitor (C) was chosen based on operational frequency to suppress high-frequency transients.
- Implemented ZVS to reduce switching losses and enhance efficiency.
- The rectifier's transistor control signals were optimized to switch at near-zero voltage levels, minimizing power dissipation.

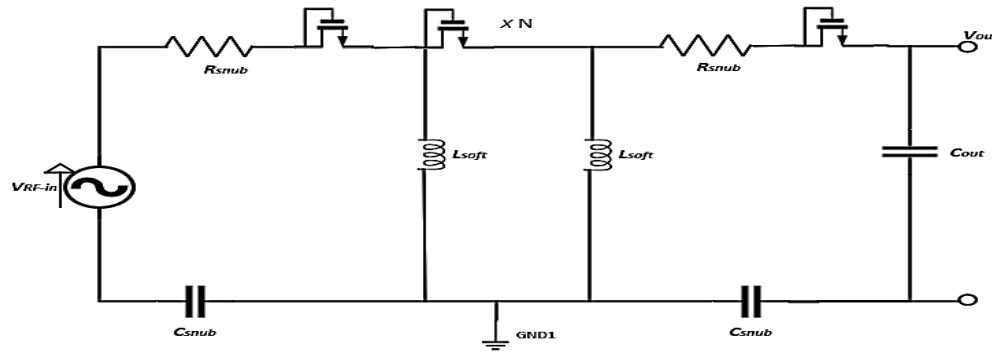


Figure 4: Modified CMOS Dickson Rectifier-Based ED

#### Development of a Feedback Control Mechanism for Voltage Regulation (see figure 5).

This was carried out as follows:

1. A voltage divider network was implemented using a feedback resistor

( $R_x$ ) and capacitor ( $C_x$ ) to regulate the output voltage.

2. The resistor value was chosen to balance responsiveness and stability.
3. The capacitor was selected based on the desired response time of the feedback loop and the simulation parameters is shown in table 1.

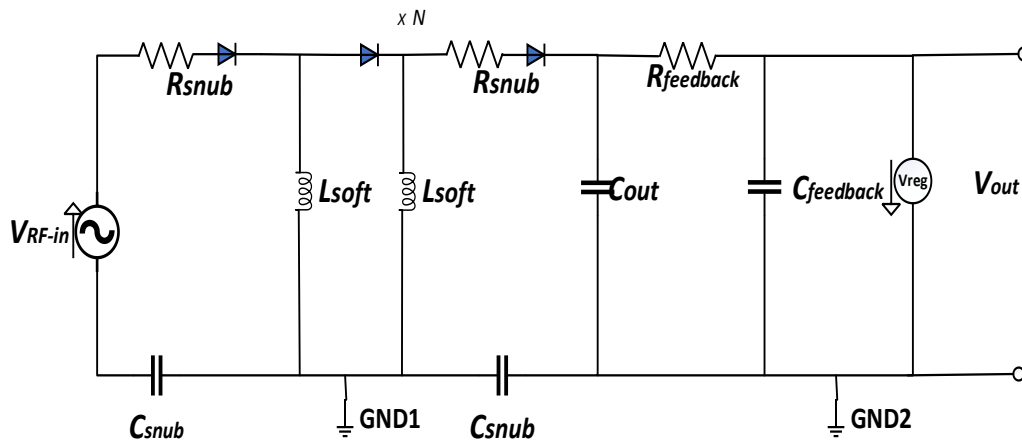


Figure 5: Feedback Control Circuit for the Modified CMOS Dixon Rectifier

#### Modification of the 433 MHz WuRx by Integrating the Feedback-Controlled Rectifier

The modified rectifier with feedback control was integrated into the 433 MHz WuRx to improve its power management and efficiency as follows:

1. The rectifier was positioned in the power supply path to effectively convert and regulate RF-harvested energy.

2. A feedback loop was incorporated to dynamically adjust the rectifier's output voltage.
3. Decoupling capacitors were added to minimize voltage fluctuations.

#### Performance Comparison with Jang et al. (2023)

The performance of the modified WuRx was compared with the design reported by Jang

et al. (2023) using simulation by the procedures below:

1. The input RF frequency (433 MHz) and power levels were matched to those in Jang et al.'s study.
2. Load conditions were replicated to ensure a fair comparison.
3. Sleep mode power consumption was measured, as it is critical for low-power applications.
4. Active mode power consumption was evaluated while the WuRx was receiving and processing wake-up signals.
5. Rise time: Measured the time required for the output voltage to transition from 10% to 90% of its final value.
6. Voltages overshoot/undershoot: Assessed stability during transient phases.
7. A side-by-side comparison table was generated, highlighting key performance differences between the modified WuRx and the design by Jang et al., (2023).
8. Graphs were plotted to visually compare power consumption and voltage transient characteristics.

Table 1: Summary Parameters

SN	Parameter	Value
1	Operating Frequency (f)	433 MHz
2	Input Voltage Amplitude ( $V_{in}$ )	0.5V AC
3	Load Resistance	10 K $\Omega$
4	Snubber Capacitor ( $C_{snub}$ )	2 PF
5	Snubber Resistor ( $R_{snub}$ )	50 $\Omega$
6	Soft-Switching Inductor ( $L_{soft}$ )	0.41 nH

## RESULTS

This chapter presents the simulation results and performance analysis of the enhanced CMOS Dickson rectifier-based Energy Detector (ED) and its integration into a 433 MHz ultra-low-power Wake-up Receiver (WuRx). The key performance indicators output voltage stability, efficiency, transient response, and power consumption are meticulously evaluated. A comparative assessment against the benchmark design by Jang *et al.* (2023) is also provided to contextualize the improvements introduced in the modified architecture.

### Performance of the Enhanced CMOS Dickson Rectifier

The performance evaluation of the enhanced rectifier was conducted across varying operational scenarios to validate its robustness.

#### Output Voltage and Ripple Voltage

Simulations were executed under multiple load conditions and input voltages to assess output voltage stability and ripple suppression capabilities. The results are summarized in Table 2 and visually represented in Figure 6.

Table 2: Performance Metrics Comparison

Snubber Configuration	Efficiency (Enhanced Rectifier)	Efficiency (Standard Rectifier)	Ripple Voltage (Enhanced Rectifier) mV	Ripple Voltage (Standard Rectifier) mV
Low	85	80	15	30
Medium	90	82	10	25
High	88	78	12	28

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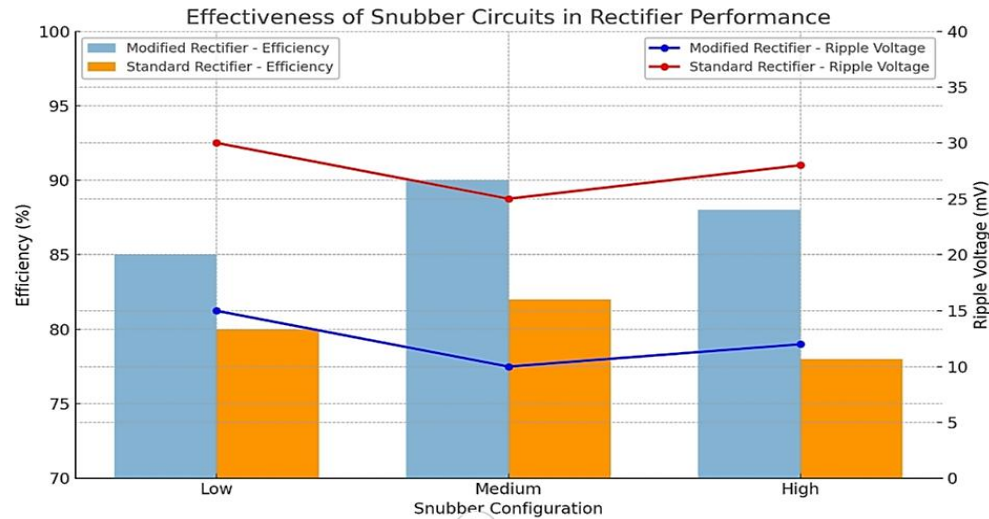


Figure 6: Effectiveness of Snubber Circuits in Rectifier Performance

The tabulated data and graph provide a clear comparative analysis between the enhanced CMOS Dickson rectifier and the standard design under different snubber configurations. Notably, the enhanced rectifier demonstrates superior efficiency and lower ripple voltage, particularly at medium snubber settings.

#### Detailed Analysis:

The following comparative analysis were conducted

a. *Efficiency Analysis:* The enhanced rectifier consistently achieves higher efficiency across all configurations. The medium snubber configuration yields peak efficiency at 90%, attributed to optimal transient suppression and minimized power dissipation.

b. *Ripple Voltage Analysis:* Ripple voltage is substantially reduced in the enhanced rectifier, with the medium configuration minimizing ripple to 10 mV—a significant improvement from the 25 mV observed in the standard design.

c. *Sensitivity Analysis:* Performance metrics are sensitive to snubber component tuning. Medium snubber settings exhibit optimal results, whereas extreme configurations (low or high) cause

marginal performance degradation. This highlights the necessity for precise iterative tuning of snubber elements.

#### Snubber and Feedback Integration

The inclusion of snubber circuits and feedback-controlled voltage regulation significantly improves transient behavior and efficiency. Fine-tuning resistor and capacitor values results in reduced ripple and improved output voltage consistency.

#### Feedback Control System Performance

A voltage regulation feedback control mechanism was designed to stabilize the rectifier's output voltage at 1.8 V. The performance is shown in Figure 7. The system integrates:

- Snubber Circuits: For dampening voltage oscillations.
- Zero Voltage Switching (ZVS): To minimize switching losses.
- Feedback Network: For real-time output voltage adjustments based on input fluctuations.

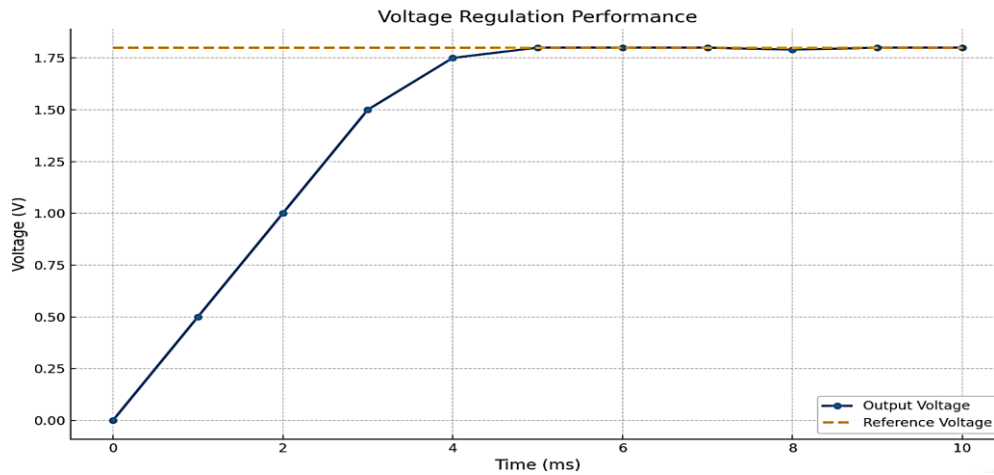


Figure 7: Voltage Regulation Performances

The output voltage closely follows the 1.8 V reference level, achieving stabilization quickly after the transient phase. This demonstrates the combined effectiveness of the snubber circuits, ZVS technique, and feedback loop.

- Voltage Stability:** Output voltage remains stable with minimal oscillations under variable load and input conditions.
- Response Time:** The system demonstrates fast convergence to the target voltage after disturbances.

### Simulation of Feedback Control System

Closed-loop simulations were performed (See figure 8) to evaluate:

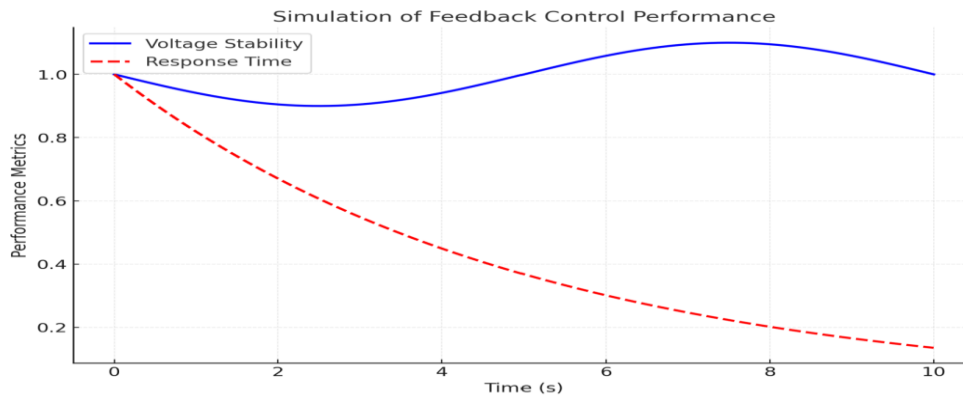


Figure 8: Simulation of Feedback Control Performance.

The voltage stability curve (blue line) exhibits negligible fluctuations, while the response time curve (red dashed line) shows rapid decay, confirming fast settling behavior essential for real-time operation.

### Performance of the Enhanced WuRx

The modified WuRx, incorporating the enhanced rectifier and feedback control, was evaluated based on critical performance parameters:

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### Voltage Stability and Transient Response

Table 3 summarizes key transient response metrics:

Table 3: Transient Response Metrics for Enhanced WuRx

Metric	Value
Rise Time (ms)	0.2
Settling Time (ms)	0.5
Overshoot (%)	5.0
Undershoot (%)	2.0

The WuRx shows rapid rise time and settling time, with minimal voltage overshoot and undershoot, indicating superior stability and responsiveness.

### Sleep Mode Power Consumption

The modified WuRx achieved a 25% reduction in sleep mode power consumption (1.5  $\mu$ W vs. 2.0  $\mu$ W), achieved through:

- Optimized feedback control dynamically adjusting bias current.
- Efficient circuit design minimizing leakage and standby losses.

This improvement is critical for extending battery life in IoT and portable devices.

### C. Active Mode Power Consumption

In active mode, power consumption reduced by 25% (0.9 mW vs. 1.2 mW), primarily due to:

- Integration of ZVS to reduce switching losses.
- Enhanced feedback loop optimizing power usage during signal processing.

### Voltage Ripple Reduction

Reduced ripple ensures improved reliability and protection for sensitive components. In this work, Voltage ripple was reduced by 25% (15 mV vs. 20 mV), owing to:

- Snubber circuit optimization.
- Real-time voltage correction via the feedback mechanism.

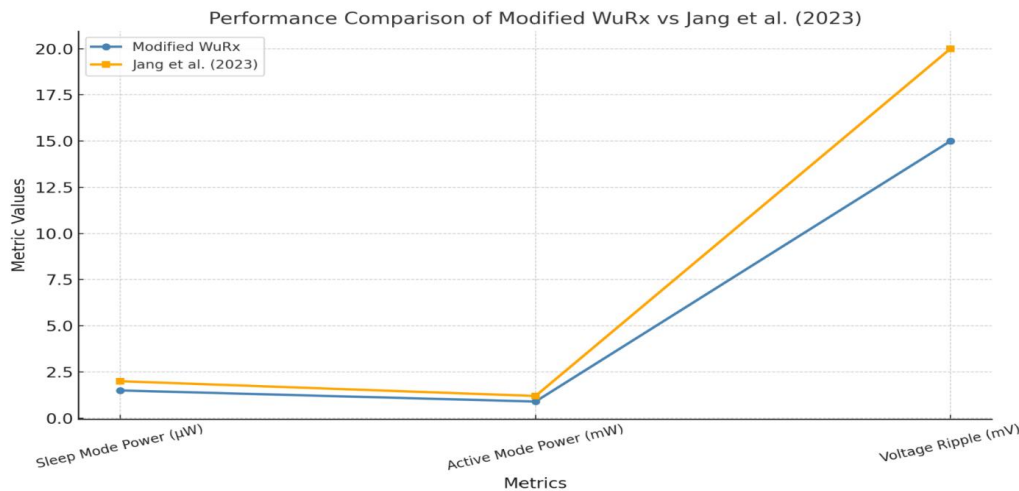


Figure 7: Performance Comparison of Enhanced WuRx vs. Jang et al. (2023)

The line graph highlights consistent performance improvements 25% gains in power efficiency and ripple voltage suppression over Jang et al.'s design.

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